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Claims

[c1] A method for manufacture of an integrated circuit having structures formed in respective first and second areas thereon, said method comprising steps of
reducing height of structures in said first and second areas,
removing a material from said first and second areas simultaneously or sequentially, and replacing said material removed from said first and second areas with a first material in said first area and a second material in said second area, respectively, one of said first and second materials being an isolation material,using a polysilicon block-out mask or a block-out mask having two layers of different materials to protect one of said first and second areas to separately process the other of said first and second areas,
planarizing said first and second materials to provide a planar surface, and
completing said integrated circuit.

[c2] The method as recited in claim 1, wherein said isolation material is an array top oxide.

[c3] The method as recited in claim 1, wherein a polysilicon

hard mask is used to mask said second area.

[c4] The method as recited in claim 3, wherein said polysilicon hard mask comprises a single layer of polysilicon.

[c5] The method as recited in claim 1, wherein a polysilicon hard mask is used to mask said first area.

[c6] The method as recited in claim 5, wherein said polysilicon hard mask comprises a single layer of polysilicon.

[c7] The method as recited in claim 1, including the further step of depositing a nitride liner prior to said step of depositing said isolation material.

[c8] The method as recited in claim 1, including the further step of
equalizing heights of structures in said first and second areas by etching prior to said planarizing step.

[c9] The method as recited in claim 1, wherein said integrated circuit is a memory device, said first area is a memory array area and said second area is a support area.

[c10] The method as recited in claim 1, wherein said integrated circuit includes an embedded memory, said first area is a memory array area and said second area is a support area.

[c11] The method as recited in claim 1, wherein said planarizing step includes
applying a planarizing material over said structures in said first and second areas and said first and second materials, and
non-selectively etching said planarizing material, said first material, said second material and said structures.

[c12] A method for planarizing a surface having structures formed thereon and an additional layer of material covering said surface and said structures formed on said surface, said method including steps of
applying a planarizing material to said layer of material to form a substantially planar surface above said surface having structures formed thereon, and
performing a non-selective etching from said substantially planar surface to a said predetermined structure formed thereon.

[c13] The method as recited in claim 12, including the further step of
performing end point detection to detect a material interface for determining termination of said step of non-selective etching.

[c14] A method as recited in claim 12, wherein

said structures have a first average height in a first area of said surface and structures of a second average height greater than said first average height in a second area of said surface, said method comprising the further steps of

etching said structures of said second average height to an average height substantially equal to said first average height,

subsequent to said etching step, applying a planarizing material to said first and second areas of said surface and covering said structures remaining in said first and second areas whereby a surface of said planarizing material is substantially planar, and

performing said step of non-selectively etching said planarizing material and structures overlaid by said planarizing material to completely remove said planarizing material and form a planar surface.

[c15] The method as recited in claim 12, wherein said step of non-selective etching includes removal of a nitride liner below said layer of material.

[c16] A method for planarizing a surface of a body of material, said method including steps of

applying a planarizing material to said body of material to form a substantially planar surface, and

performing a non-selective etching from said substan-

tially planar surface to a point on or within said body of material.

[c17] The method as recited in claim 16 in combination with a top oxide early process for forming an integrated circuit.

[c18] The method as recited in claim 16 in combination with a top oxide nitride process for forming an integrated circuit.

[c19] The method as recited in claim 16 in combination with a top oxide late process for forming an integrated circuit.

[c20] The method as recited in claim 16 including the further step of adjusting height of a structure on a differentiated area of said body of material.